UBM Electronics

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Test & MEASUREMENT WORLD

THE MAGAZINE FOR QUALITY IN ELECTRONICS

Rule out thermal issues during development

Real-time monitored thermal-cycling techniques can improve reliability prediction for packaged modules.

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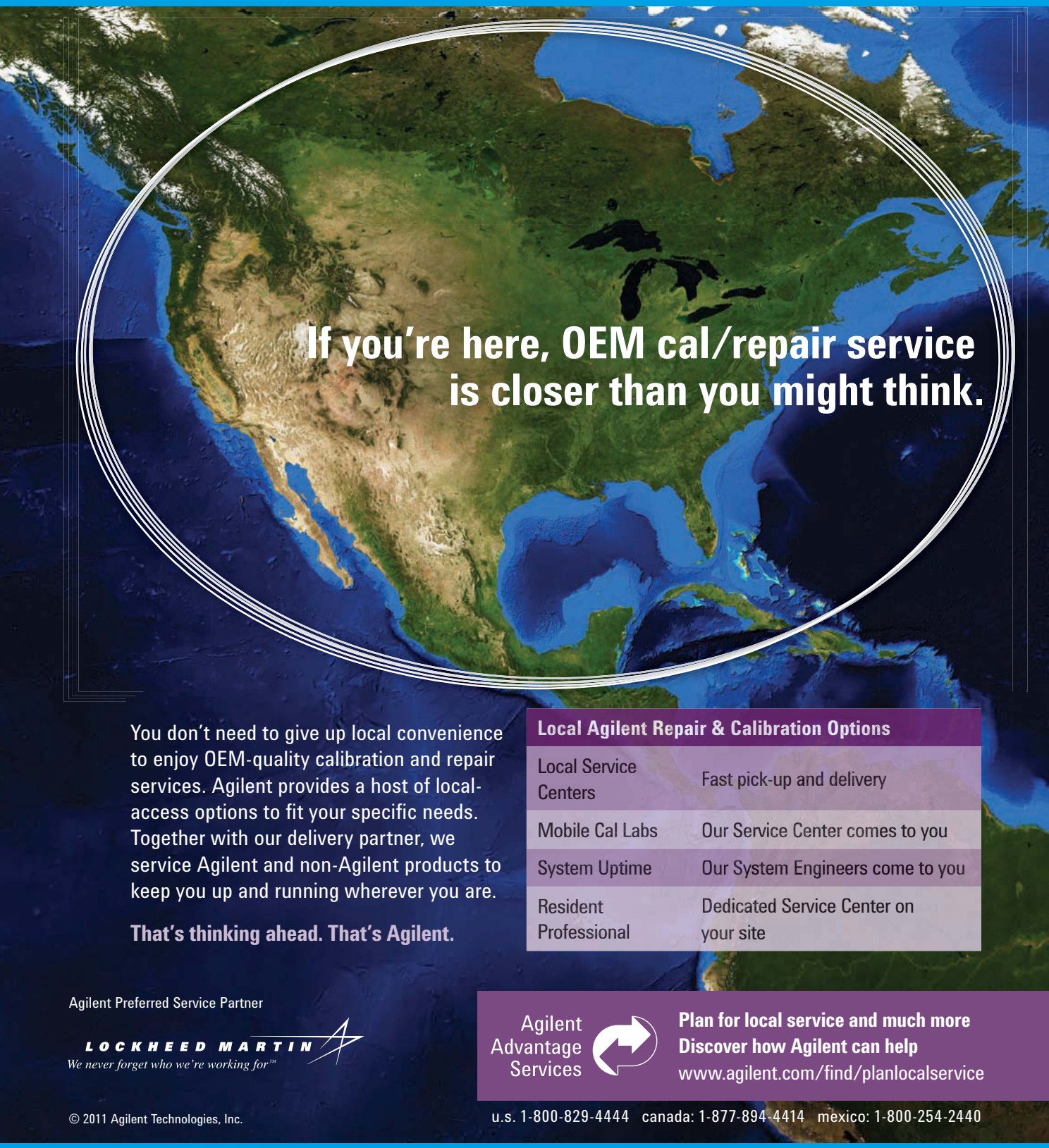

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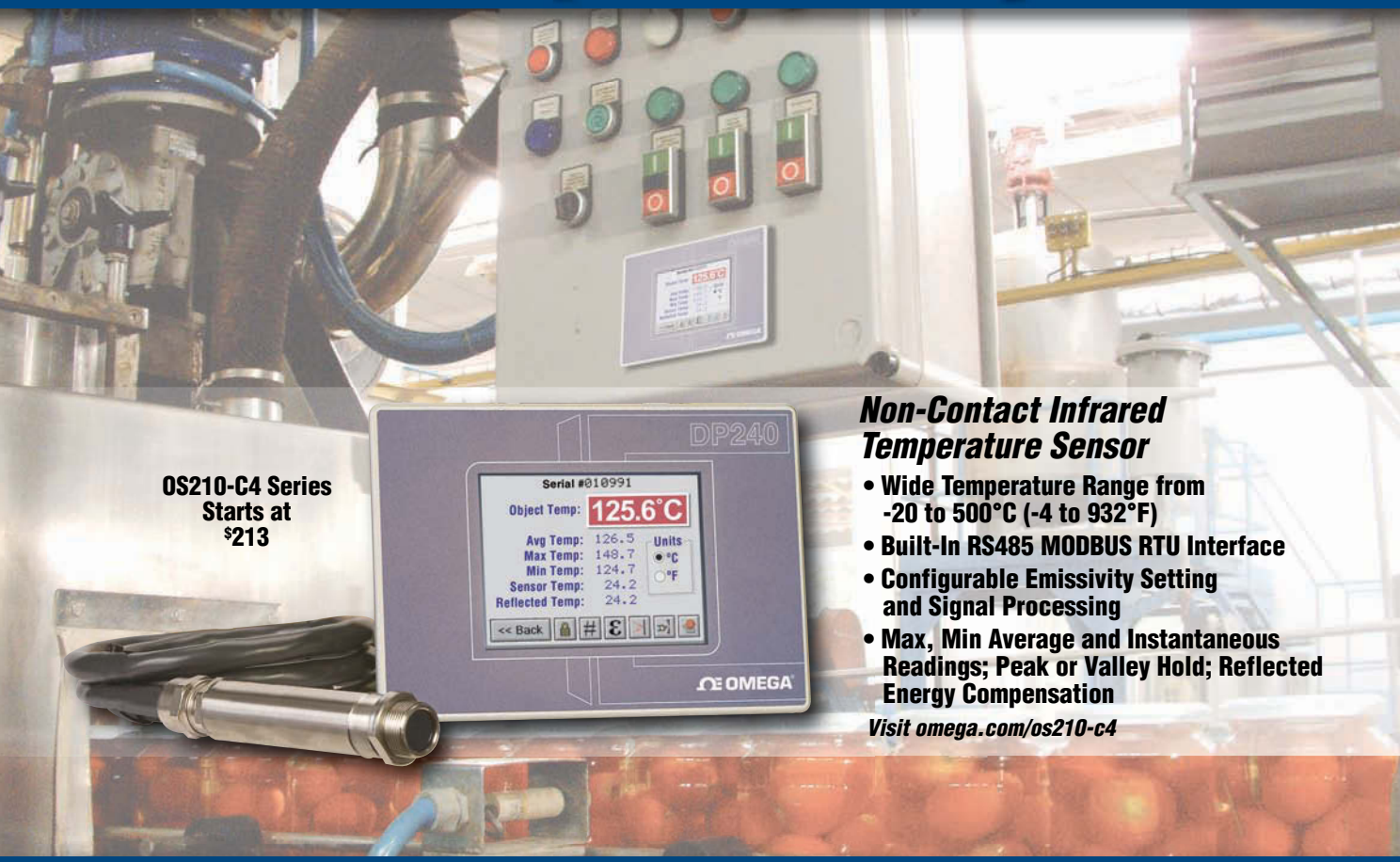

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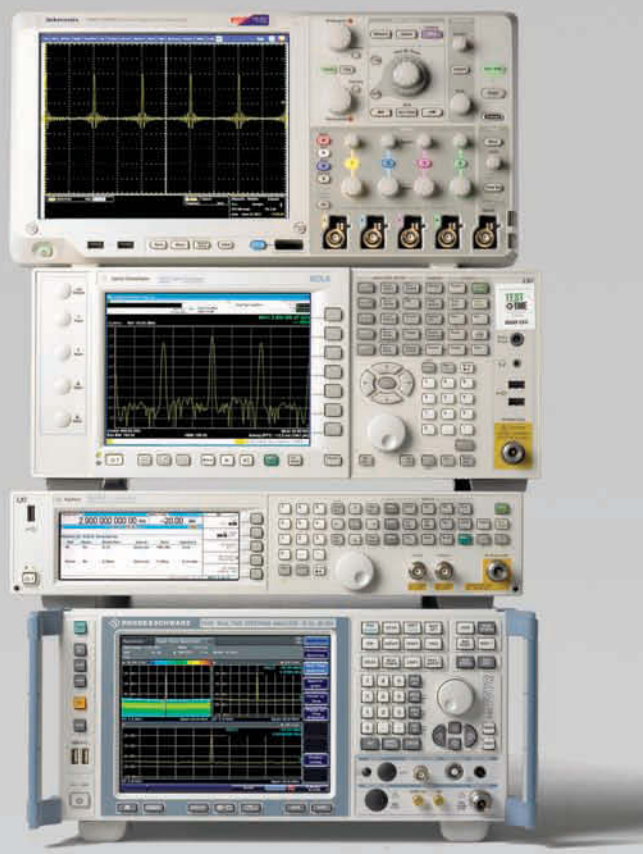

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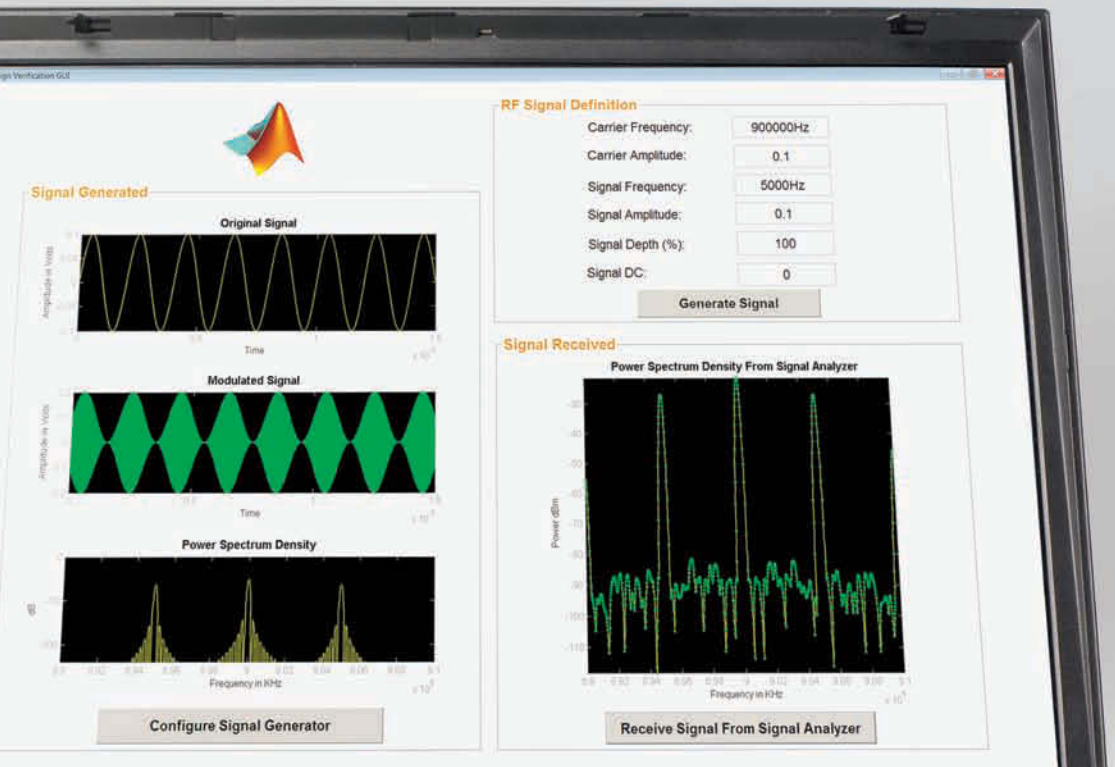

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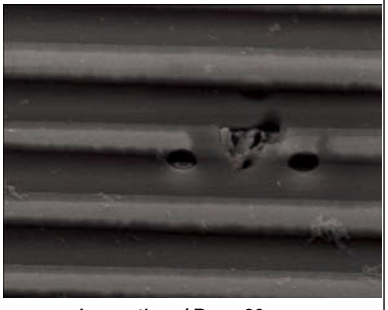

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Test & MEASUREMENT WORLD®

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VOL. 32 NO. 3

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VIEWPOINT

Online now at TMWorld.com

Check out these exclusive features on the *Test & Measurement World* Website:

Deterministic jitter for receiver tolerance testing

Join the conversation! Ransom Stephens says that the idea behind receiver tolerance testing is to submit the receiver to "the worst case but compliant" stress. Most standards require a deterministic jitter in a combination of sinusoidal jitter and intersymbol interference.

bit.ly/yVOIIO

OFCNFOEC: Talk moves past 100G

Everywhere you look, optical transceiver makers, test equipment makers, and component makers are pushing 40G and 100G data rates. At OFCNFOEC, the "Lighting up the data center" Service Provider Summit made it clear that many data centers are moving to 40G because of lower costs than implementing 100G.

bit.ly/AjRV1Q

Oscilloscope memory depth: when bigger is not always better

Oscilloscope memory depth is an often misunderstood concept. Richard Markley of Agilent Technologies explains what scope memory is and discusses the tradeoffs of memory in different scope architectures.

bit.ly/vZi877

Is DLNA certification needed?

The Digital Living Network Alliance certifies products that provide interoperable multimedia solutions. Such products can be appliances, computers, network devices, televisions, smartphones, or tablets.

bit.ly/z5vj31

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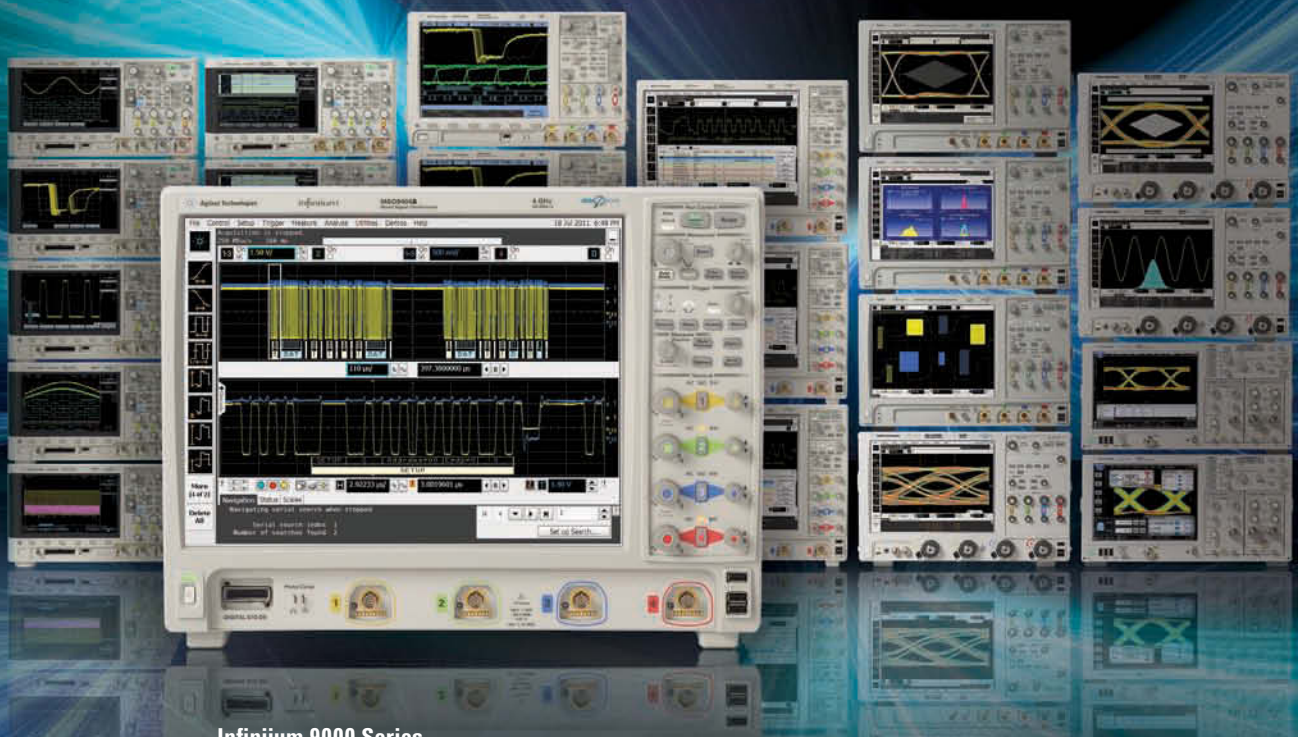

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A UBM Electronics Publication

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Testing opportunities

About 17 years ago, I joined the high-tech world of electrical engineering. Since then, I have been fortunate enough to get some of the first glances at new semiconductor processing materials and technologies, like SiGe and GaN.

I worked closely with the engineers who designed the equipment to measure how much copper was being deposited on wafers and to determine the thickness of the oxide layers on a wafer. I made my way around clean rooms, put together instruments, and saw the latest probes, lithography, and deposition tools. I played with the newest and most secret oscilloscopes, multipath fading emulators, and spectrum analyzers and saw the wicked-cool military technology that was being turned into commercial applications.

Let me know if there is a topic or product type you would like to know more about.

Of course, even if I could talk about some of these secrets, much of what I have seen, heard, learned, and written about makes no sense to my extended family at Thanksgiving dinner, who I still think have just a very vague concept of what I do all day. Now, after years of rambling around the world as a freelance writer, I have happily joined the team at *Test & Measurement World*. Long a part of the UBM family as the editor of "RF & Microwave Designline," "Memory Designline," and "Test & Measurement Designline," I always seem to find my way back to test. And I am pleased to be working to bring you technical features, news, products, and information that aim to help you with your latest projects.

For example, this issue's cover story is from a team of engineers at RFMD who describe how monitored temperature cycling can speed up electronic module reliability testing. This issue also includes a technical feature from Mark Woolley and Jae Choi at Avaya about how the combination of scanning electron microscopy and energy dispersive x-ray spectroscopy can help determine the cause of TFT LCD failures.

In addition, we have an article from Brad Quinton of Tektronix that explains how to debug a system-on-a-chip using embedded instruments, with a special focus on how the integration of hardware and software views can lead to faster system debugging.

Whatever your test challenge, now is an excellent time to be involved in the design of electronic components and systems. Manufacturers of test equipment are driving the cutting edge of what can possibly be tested, and they are achieving record results and throughput in simulation, prototyping, manufacturing, production, and field test. This, in turn, is making leading-edge devices, components, and systems possible that are being used to enable even better test equipment.

So, from the clean room to the lab, the board room to the trade show floor, and the classroom to the cell tower, I'm now part of an excellent team of editors who are on the case for you. I look forward to working with you, and thanks for all of the warm welcome messages I have already received.

Please let me know if there is a topic or product type you would like to know more about (janine.love@ubm.com), and I will endeavor to chase it down for you. In the meantime, I hope you enjoy this issue, and don't forget to sign up for our newsletters, follow us on Twitter (TMW_Community) and check out what we have for you on www.tmworld.com. T&MW

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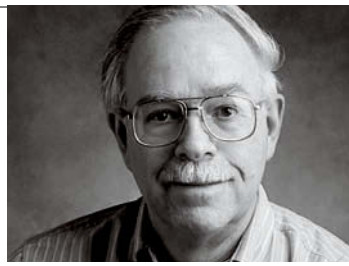
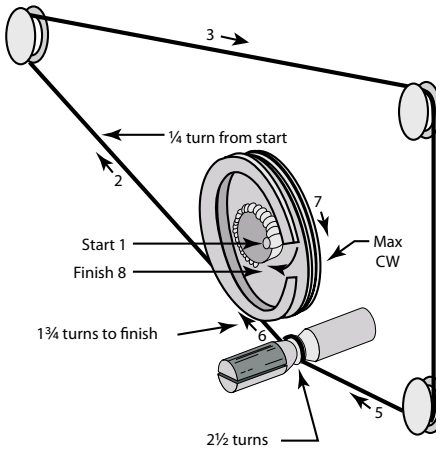


String 'em up!

With apologies to Fred Foy, Brace Beemer, and the writers of "The Lone Ranger" radio program, "Return with me now to those thrilling days of yesteryear. The Analog Dial Pointer rides again!"…or not, if you're unable to repair the damned thing.

If you've never peered inside the cabinet of a 1950s-vintage radio, you may have missed seeing one of the most frustrating and diabolical technological innovations of the electronic age—the dial-cord drive. The dial-cord drive's task is simple: translate a control's rotation into actuation of an electronic component while providing a visible analog indication of the component's setting.

In an AM broadcast-band receiver, twisting the tuning knob rotates the tuning capacitor and moves a pointer along a frequency scale. The Depression-era advent of molded plastic cabinets and miniaturized components made table-model radios popular, and dial-drive designs proliferated as cabinet stylists' imaginations ran wild. Complex drives may include a 2- to 3-ft length of dial cord, several miniature pulleys, one or more tension coil springs, and an indicator dial or pointer. A few test instrument designs also include dial-cord drives.



In practice, dial-cord drives suffer from a number of failure modes: cords slip and break, and tension springs stretch, often as a result of users' overtorquing controls. Over time, extensive use wears and polishes pulleys' surfaces, which results in slippage. Mice residing in stored equipment use dial cords as nesting material.

Repairing a broken drive requires a supply of dial cord—typically comprising a nonstretchable core overbraided with nylon, or in some applications a bronze or stainless-steel cable. Dial cord comes in several diameters, and selecting the wrong size can prevent a successful repair. Finding replacement tension springs may prove challenging, but don't overlook junked ink-jet printers as a source. Helpful tools and supplies include a bottle of rosin dissolved in alcohol (an antislippage compound) and a collection of hemostats and forceps (available in outdoor-supply stores that cater to fishing-fly crafters). You'll need a restringing diagram (if available), manual dexterity, patience… and the persistence of the Lone Ranger! T&MW

To read past Test Voices columns, go to www.tmworld.com/testvoices.

SOURCES AND SUPPLIES

If you're determined to repair Grandma's table radio or a 1960s-vintage sweep generator's nonworking slide-rule frequency dial, the following sources (among others) of dial-drive belts, cables, cords, and tension springs may prove helpful (hobby-supply and hardware stores also may offer small tension springs):

www.adamsradio.com

www.dialcover.com

Manufacturers' service manuals generally offer the most detailed dial-cord repair diagrams. Howard W. Sams Co. published two compilations of dial-drive configurations that cover older radio receivers but lack detailed information:

books.google.com/books?id=lhpTAAAAMAAJ&dq=editions:UOM39015006086865

books.google.com/books?id=rBpTAAAAMAAJ&dq=editions:UOM39015006086865

When dial-drive repair is impractical, consider substituting a frequency counter. To accommodate a superheterodyne receiver's intermediate frequency, the counter design must include a frequency offset, as described in this example:

www.norcalqrp.org/fcc1.htm

An Internet search will yield frequency-counter designs that can be modified. Here are two examples:

cappels.org/dproj/30MHzfmeter/30MhzFmtr.html

www.qsl.net/zl1bpu/MICRO/COUNTER/index.htm

After struggling with a dial-cord replacement, tip your hat in salute of the patron saint of dial-drive designers—engineer and cartoonist Rube Goldberg:

www.rubegoldberg.com

…and the persistent Lone Ranger:

www.lonerangerfanclub.com/radio.html

JDSU introduces network-monitoring probe

During the Mobile World Congress 2012 (February 27 to March 1, Barcelona, Spain), JDSU exhibited its PacketPortal network-monitoring solution. While most monitoring solutions use large, power-hungry probes, PacketPortal uses a small ASIC that reside inside the pluggable optics of network equipment. The first generation of PacketPortal captures network data from optical transceivers that are about the size of a USB memory stick.

PacketPortal takes advantage of the fact that network equipment has adopted commercial pluggable optics, typically gigabit optical Ethernet based on the SFP (small form-factor pluggable) standard. JDSU designed an ASIC that resides inside the SFP device and monitors the traffic on the GbE port. It has flexible filtering and can be set to monitor video, voice, and other traffic. There's no need for external hardware—a manufacturer can insert the ASIC right into a piece of network equipment.

To communicate its measurements back to a network-monitoring server, PacketPortal uses the occasional gaps and spare bandwidth that exist in GbE: The device slips the measurement data back into dead spots in the IP stream, to be extracted by the server and the PacketPortal software. The technique allows extreme scalability and enables users to monitor nearly any point on the network edge. www.jdsu.com. *Larry Desjardin, Contributing Editor*

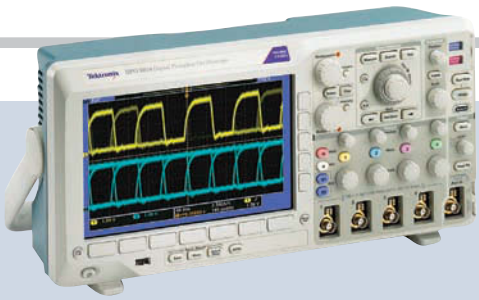
iNEMI planning MEMS test initiatives

iNEMI (International Electronics Manufacturing Initiative) has begun driving two collaborative efforts that will focus on reliability and testing issues for MEMS technologies. Using information gathered for the 2011 iNEMI Roadmap, the organization has identified several issues that must be addressed for the MEMS industry to move forward. As a result, iNEMI is now planning to develop new MEMS test methods and reliability methodologies.

For the test methods, a research team will focus on possible refinements for in-process testing as well as for performing tests at the process back end. For the reliability methodologies, an iNEMI team will investigate the development of generic reliability testing methods that effectively propagate key device failure mechanisms.

In addition, iNEMI is planning a one-day workshop during which participants will identify areas that could benefit from industry collaboration related to MEMS manufacturing and deployment. The workshop is scheduled for May 10 in Pittsburgh, PA. www.inemi.org.

Editors' CHOICE



Tek updates mixed-signal scope families

With six new models in its MSO/DPO400B mixed-signal oscilloscope line plus enhancements to its MSO/DPO3000 series of mixed-signal oscilloscopes, Tektronix is addressing embedded system test and debug needs at more aggressive price points. The six new MSO/DPO4000B scopes offer 1-GHz performance. Two-channel models offer 20-Mpoint record lengths, while the two- and four-channel "lite" (or "L") versions offer a 5-Mpoint record length at a starting price of less than $10,000.

The 1-GHz oscilloscopes include one 1-GHz passive probe per analog channel. This general-purpose probe features low 3.9-pF capacitive loading for visibility into the high-frequency signals found in USB 2.0 and Ethernet devices. Competitors' 1-GHz oscilloscopes often come with 500-MHz probes, requiring additional investment for testing higher-speed signals.

New upgrades for Tek's MSO/DPO3000 oscilloscopes allow engineers to simply upgrade bandwidth (up to 500 MHz) when project requirements change, rather than purchase a whole new instrument. The 3000 series also now provides support for MIL-STD-1553 and FlexRay serial buses. The DPO3AERO and DPO3FLEX modules enable triggering on packet-level information and offer analytical tools such as digital views of the signals, bus views, packet decoding, search tools, and packet-decode tables with time-stamp information.

Base prices: MSO/DPO4000B—$9990; MSO/DPO3000—$3380. *Tektronix, www.tektronix.com.*

CALENDAR

International Microwave Symposium, June 17–22, Montreal, QC. *IEEE, www.ims2012.mtt.org.*

SEMICON West, July 10–12, San Francisco, CA. *SEMI, www.semiconwest.org.*

EMC Symposium, August 5–10, Pittsburgh, PA. *IEEE Electromagnetic Compatibility Society, www.2012emc.org.*

Autotestcon, September 10–13, Anaheim, CA. *IEEE, www.autotestcon.com.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Analyze optical and electrical data streams

Editors' CHOICE

Complex modulation, used to achieve data rates of over 25 Gbps per lane, has grown as 40-Gbps and 100-Gbps links come online. In some labs, engineers are developing enough optical and electrical products to require more than one OMA (optical modulation analyzer). Seeing that trend, Agilent Technologies has developed the N4392A, a four-channel OMA with a large 15-in. screen. With a weight of 13 kg (28.7 lbs.), the N4392A is light enough to travel from bench to bench. In other words, you could find yours on a colleague's bench at any time.

The N4392A can let you view constellation diagrams and perform vector-signal analysis on an optical transmitter's output modulation. Eye diagrams let you see demodulated data streams. Because engineers can use the instrument for electrical or optical signals, it's available with an optical receiver, an electrical receiver, or both. Each receiver contains a 63-Gsamples/s ADC and an RF amplifier, which lets the instrument capture 32-Gbaud modulated signals. The optical receiver covers the range of 1527.6 nm to 1565.5 nm.

Base price: $165,000. *Agilent Technologies, www.agilent.com/find/N4392A.*

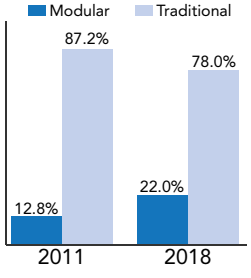
Market Trends

Demand for modular instruments on the rise in India

"Modular" is the buzzword in the Indian general-purpose instrumentation market. Because of modular instrumentation's ease of use, flexibility, low cost of test, and use of software, customers increasingly prefer modular instruments over traditional ones. While the split of the market revenues for general-purpose test equipment in India is currently 12.8% for modular instrumentation and 87.2% for traditional instrumentation, the market split is expected to change to 22.0% and 78.0% by 2018.

PXI, VXI, and AXIe are the predominant standards for modular instruments. PXI is the most-favored platform and contributes to at least 70% of the total modular instrumentation market in India. Several international and regional companies in India are focusing on developing new test equipment based on this standard.

The PXI-based instrumentation market in India registered revenues of approximately 540.0 million Indian rupee in 2011 (approximately $11.6 million US). The market is expected to grow at a compound annual growth rate of 22.3% between 2011 and 2018. The PXI platform addresses one of the problems in the instrumentation market: Instruments from different companies may have connectivity issues. The PXI platform overcomes these issues, which is one of the reasons for its adoption rate.



Modular instruments are gaining an increased share of the instrumentation market in India.

Source: Frost & Sullivan.

Introduced in 2009, AXIe is not yet available on many instruments. This market segment is expected to grow at a slow but steady pace.

While VXI was the first modular instrumentation standard on the market, it has now run the course of its life. A handful of companies still offer instruments based on this form factor, serving the needs of the aerospace and defense industry.

With an increase in efficiency and knowledge among end users about the capabilities of modular instruments, there is expected to be tremendous growth and opportunities for modular instruments in India going forward.

Sujan Sami, Research Analyst, Frost & Sullivan

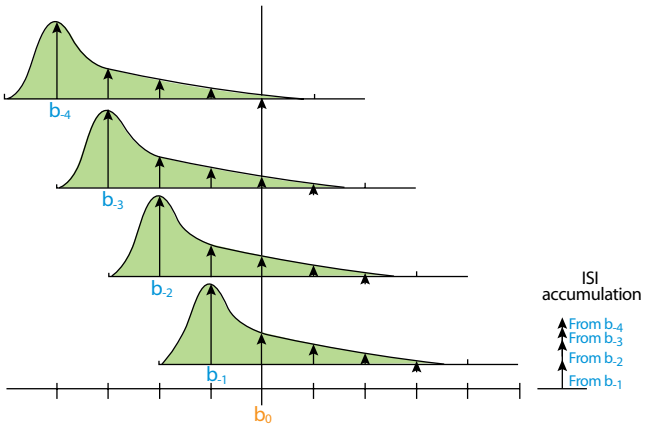
INSTRUMENTATION

Optimize digital patterns for worst-case testing

Complete validation of a high-speed serial link (28 Gbps) requires long patterns—some 2 billion bits. Long simulation run times and limitations in oscilloscope memory length make these validation tests time-consuming and difficult.

To combat the problem, engineers Masashi Shimanouchi, Mike Peng Li, and Daniel Chow of Altera studied how to optimize bit patterns and find the patterns that produce the worst-case amount of ISI (intersymbol interference) in a data stream. Shimanouchi presented the results of the group's research ("Worst-Case Patterns for High-Speed Serial Link Simulation and Measurement") during DesignCon 2012.

Because bits tend to stretch in time as they travel, energy from one bit can interfere with adjacent bits, resulting in ISI. The **figure** shows how bits overlap and how their energy can accumulate in later bits.



Energy from bits can interfere with nearby bits, called intersymbol interference.

Shimanouchi explained that you can design a short pattern of perhaps 10,000 bits to induce worst-case ISI, but only if you know characteristics of the transmission channel, with settling time being a key parameter. That's because bit patterns can cause the DC level in a channel to change. So, the Altera engineers looked for patterns that cause the greatest changes in DC level, which is a combination of long and short.

Shimanouchi also noted that the worst-case pattern for a given link, which he called "pathological worst case," might never occur in a real system. Thus, the engineers looked for patterns that, while less severe than the pathological worst case, are more likely to appear in a link.

In their study, the engineers looked at what causes worst-case eye height and worst-case eye width. These conditions occur when noise is injected in the middle of an eye, which affects height, or when noise is injected at transitions, which affects width.

They set out to design a pattern that maximized both conditions and then studied the effects of those conditions on ISI. To do that, they used spectral analysis with a short-time Fourier transform to find the channel loss versus frequency for worst-case eye height and worst-case eye width.

They measured the spectral response of the channel with and without pre-emphasis on the transmitted signals to see how pre-emphasis improves signal loss in the channel. By using these worst-case patterns, the engineers shortened test time. More work is needed to find even shorter worst-case patterns.

You can download a PDF of the engineers' paper from the online version of this article at www.tmworld.com/2012_04.

Martin Rowe, Senior Technical Editor

PRODUCT TRYOUT

Can a $129 spectrum analyzer be any good?

Every EMC or design engineer should own a spectrum analyzer. Most new models, however, are expensive, and used models are large and heavy. Until recently, these instruments have been priced too high for electronics hobbyists or engineers on a budget. Imagine my surprise when I found the RF Explorer, a handheld spectrum analyzer priced from as little as $99. Could it possibly be any good?

There are five RF Explorer models. Four are single-band units, each covering the most-used ISM (Industrial Scientific Medical) bands (433 MHz, 868 MHz, 915 MHz, and 2.4 GHz). The fifth model encompasses all bands except 2.4 GHz, but the 2.4-GHz band may be retrofitted for an extra $55. The RF Explorer uses the Silicon Labs Si4431 receiver chip (240 MHz to 960 MHz). I purchased the $129 WSUB1G, which tunes from 240 MHz to 960 MHz.

To test the RF Explorer, I attached an H-field loop probe from Beehive Electronics and started probing a crystal oscillator demo board (**figure**). The sensitivity was sufficient to display usable harmonics.

The analyzer is relatively easy to configure for frequency and span (or high and low limits) and reference level. Once the span is set, pressing the left and right keys causes the

frequency to change in half-span steps. Pressing the up and down keys changes the vertical range in steps according to the defined vertical scale. Users can automatically set and display the RBW (resolution bandwidth) by pressing the return key during a measurement. This displays the center frequency, span, and RBW. Pressing the return key once again displays the start, center, and stop frequencies.

While the RF Explorer is certainly usable as a limited EMC troubleshooting tool and for general spectrum measurements, it does have a few drawbacks. For example, the unit seems to measure about 4 dB to 5 dB low at the frequencies I tried. Ariel Rocholl of the RF Explorer site (micro.arocholl.com) acknowledges this is an issue with some frequencies and is working on a user-based calibration procedure. Despite the instrument's shortcomings, the price/performance is spectacular and may be just the ticket for cash-strapped companies who need a minimal instrument to beat down their emissions problems.

For my complete review of the RF Explorer, see the online version of this article, which also contains a list of features and specifications (www.tmworld.com/2012_04).

Ken Wyatt, Wyatt Technical Services

Probing a crystal oscillator demo board with the RF Explorer displays usable harmonics.

Rule out thermal issues during development

Real-time monitored thermal-cycling techniques can improve reliability prediction for packaged modules.

BY M. FERRARA, M. STEPHENS, L. MARCHUT, C. YANG, V. FRYAR, AND P. SCOTT, RFMD

Tools that can help identify packaging reliability risks earlier and with additional depth are becoming increasingly important. One such tool is a real-time, thermal-cycle reliability test in which the module package is monitored with a resistance daisy-chain methodology during temperature cycling. This test provides immediate real-time failure feedback and enhanced failure signature information and has proven to be a valuable method for capturing the early stages of a module mechanical failure at temperature extremes.

Today's electronic module packages can integrate several active and passive components within one device, providing simpler board design, reduced component inventory, and reduced repair costs (Ref. 1). Yet, as module footprints continue to reduce in size while increasing in packing density, finding ways to test them becomes challenging. Choices in the module material set, component variables, and substrate considerations all play substantial roles in determining the overall package reliability, and they ultimately determine which test methodology would be best to verify reliability.

Over the past decade, the industry has moved from relying on pass/fail test methods toward using design-for-reliability tests that focus on uncovering and analyzing potential problems at an earlier stage. A facet of this is the increased emphasis on the test-to-failure approach (particularly in the development stages) for certain packaging-related tests. Additionally, there is increased emphasis on extracting more meaningful data from standard fixed-duration tests, such as TC (temperature-cycling) tests.

Temperature cycling

From the perspective of reliability test, TC stress testing has traditionally been a "pass or fail" test where a thermal-cycle stress is induced and functional units are subsequently removed from the TC stress (either as a "loose" piece or attached to a carrier board) for verification of post-TC electrical-test functionality.

In general, a TC stress profile involves the following parameters:

- high extreme temperature (T_{MAX});
- low extreme temperature (T_{MIN});
- temperature change (T), where $\Delta T = T_{MAX} - T_{MIN}$;
- ramp rates; and
- dwell times at extreme temperatures.

The lifetime of a PA (power amplifier) module, in particular, can be significantly affected by these parameters. TC tests can be used to characterize product capability and accelerate failure modes (e.g., die crack, via crack) during initial technology development, product design verification, and product qualification (Ref. 2).

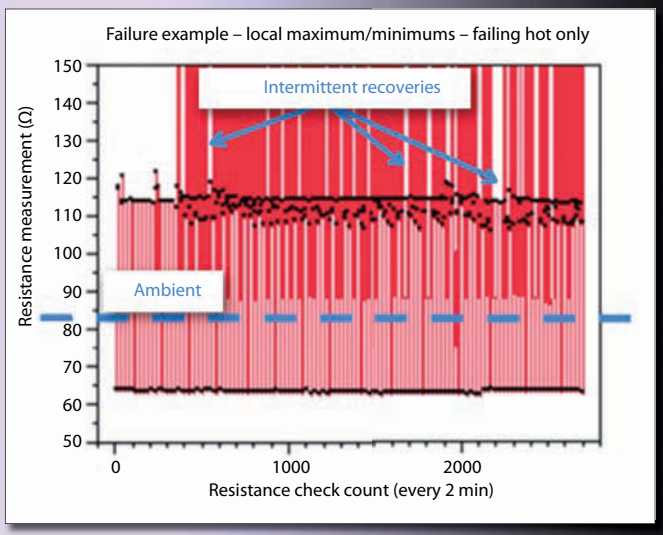


FIGURE 1. In this module under test, a full set of failing data (300-cycle span) fails to the hot side. The data indicates some intermittent recovery time periods occurring well above ambient.

Monitored temperature cycling

As an enhancement to existing TC stress methodologies, implementing a monitored daisy-chain in real time during the TC stress can help determine if any intermittent failures are beginning to occur. As a result, designers can be alerted to a failure immediately without the need for post-TC electrical test. A monitored test includes:

• *Event detection.* In order to capture a significant resistance change in real time, the event-detection capability called for in monitored drop-shock testing, for example, requires very-high-speed data acquisition over a short period of time (typically a 0.05-ms event-detection capability), with data captured for approximately a 1-s window during impact. For the monitored TC stress event detection, however, this level of high-speed capability is not necessary or even desired. The failure mechanisms associated with TC stresses tend to be very slow to develop and will not change quickly from passing to failing and back to passing.

A switch matrix that can "ping" all of the modules under test on the scale of once per minute, for example, is more than adequate. The slower speed of this event detection also reduces the amount of "streaming" data that needs to be sorted and evaluated.

The switch-matrix output can be delivered to a software interface where the resistance data can be compiled, analyzed, and flagged for exceeding resistance thresholds (which might

be set to a value anywhere between 1000 Ω and 5000 Ω). Note that a normal passing module exhibits a resistance change range that is in lock step with the thermal oscillations (thermal coefficient of resistance). For example, the normal resistance range oscillates naturally between 64 Ω (cold) and 113 Ω (hot).

• *TC profile.* Any type of temperature cycle profile can be used in conjunction with monitored TC testing. Industry standards such as JEDEC Standard JESD22-A104D (Ref. 3) or any other customer specification could be used as a reference or guideline.

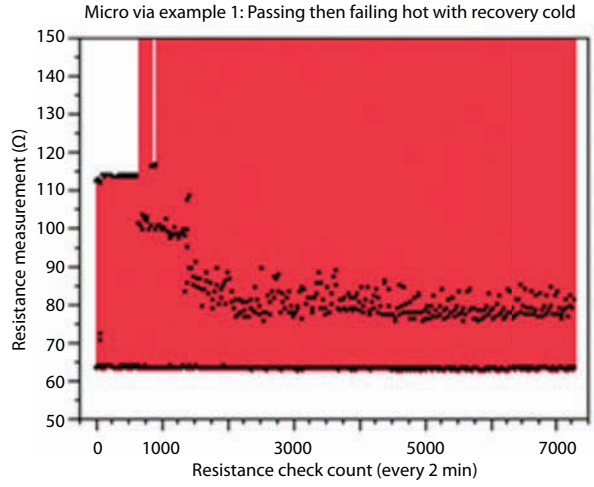


FIGURE 2. For this module, failure occurred after the 800-resistance check mark. In addition, local maximum data points were monotonically degrading over time.

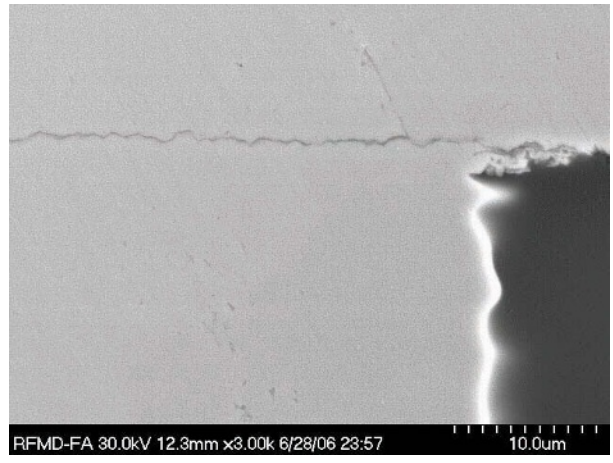


FIGURE 3. This image of a failure-analysis result indicates the root cause is a separation of a micro via within the module laminate.

Monitored TC data analyzed

Once it is captured, raw data (channel, resistance, count, time, and so forth) can be exported, analyzed, and graphed within a software package such as SAS Institute's JMP software. Within JMP, a "local" maximum and minimum algorithm can be used to strip away the "normal" interior data, allowing designers to focus on potential failure data (major resistance changes or opens).

By capturing resistance data throughout the thermal cycle, it is possible to detect failures that first develop at extreme temperatures. In contrast, many additional cycles may need to be completed before the failure would present itself in an ambient, post-TC electrical test.

Furthermore, we have observed several cases in which a failure recovered prior to the module returning to ambient thermal levels within the cycle, suggesting that the probability of detecting the failure in a post-TC electrical test may be low.

For example, the monitored TC method allowed early detection of a micro via separation that may have been difficult to recognize using traditional TC testing methods. This failure mode consistently first appeared in the hot phase of the cycle, but it would recover as the cycle re-approached ambient temperatures and remained recovered throughout the cold phase (**Figures 1** and **2**).

In a related example, presumably as the separation at the interface became more pronounced with continued thermal stress, the failure would begin to "go open" at lower and lower temperatures and eventually settle at a minimum steady-state temperature (**Figures 2** and **3**). This temperature may or may not be below ambient. And in some cases (when failure analysis attempted to recreate the failure mode), a hot plate was needed to isolate the failure.

Another example offered early detection of a second type of failure mechanism, the separation of a SAW (surface acoustic wave) filter from the under-bump metallurgy (the metal layer under the solder connection). Unlike the previous example, this problem presented itself in the cold phase only and returned to normal when transitioning into the hot phase of the thermal cycle (**Figures 4** and **5**).

Once again, the progression of failure can be characterized from the data overlaid with short bursts of recovery. The failure still exists during these recoveries, but it is masked by a temporary mechanical connection. Such a failure may have been delayed or missed entirely during traditional post-TC electrical testing. As a result, even if some failures were detected, the seriousness may have been underestimated because the failure percentage would be lower than actual for the sampling population.

Whether the signatures of the failure detected in monitored TC could be used to identify specific failure modes is still undetermined. It is clear from these two case studies, however, that some general assumptions about the failure mode type can be made.

Overall, monitored TC is an effective accelerated package reliability test method for electronic module packaging. The method is particularly useful during development phases when designers must establish confidence in new packaging technologies. The ability for monitored TC to detect a fail-

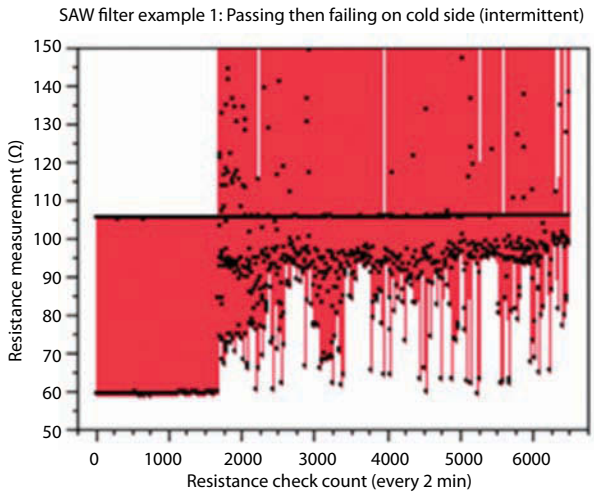


FIGURE 4. This daisy-chain module indicates normal resistance and then begins to fail on the cold side. Intermittent recovery is sporadically evident.

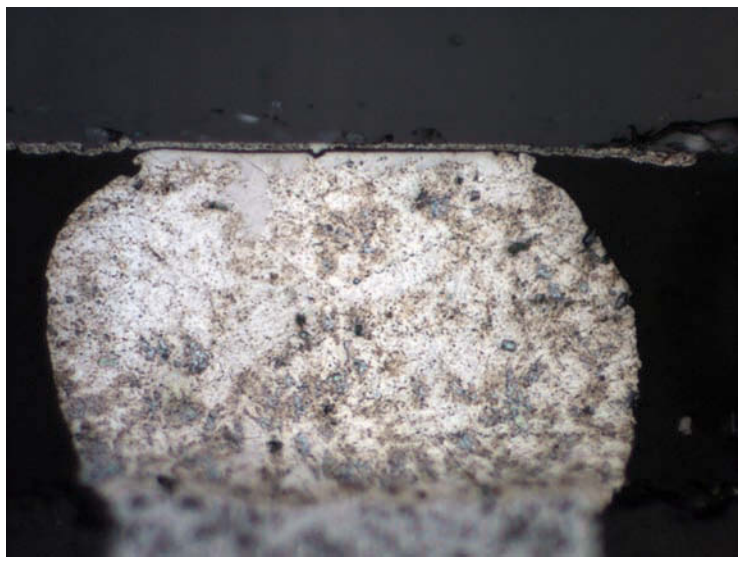


FIGURE 5. The cause identified in failure analysis of the module in Figure 4 was a separation of under-bump metallurgy for a SAW filter in the module.

ure at the precise cycle count at which it begins to occur is an advantage for earlier detection as well as for accurate statistical analysis. Detailed data regarding the signature of the failure and progression of the failure can be valuable in assisting failure-mode determination and reducing failure-analysis time. T&MW

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Design test software for platform independence

By using abstraction layers when developing code, you can write test software that will have a long life.

BY ROB MARQUARDT, MARQUARDT TEST SYSTEMS

A test system's expected lifetime often exceeds the production lifetime of its individual components, making it difficult for a company to build an identical test system or replace a failed instrument. Even if the instruments don't fail, you might want to use new test hardware that can do a better job than old equipment, but you might be forced to stick with what you have because of the investment that would be required to update the system software: The cost of rewriting and validating functioning test code can kill a system upgrade.

Thus, engineers often do everything possible to extend the life of the obsolete equipment until that becomes too costly or impossible, at which point a big investment in new equipment and new software is required. Then, the cycle repeats.

When designing a test platform, you should provide a hardware-abstraction layer similar to the one used on PCs that lets Windows run on various hardware topologies. Such a layered approach lets test sequences and test routines run without modification across multiple test platforms. If you use such a hardware-abstraction layer, the same test could be run on a platform with hundreds of switch points and on a custom test setup with no switching at all. A test system I designed in 1995 still runs today, in part because of its layered software design.

Part of the project's first goal was to allow for test fixture reuse even if the ITA (interface test adapter) changed. I recommend keeping the same ITA in a new test-system design to allow for reuse of the existing test fixtures. ITAs can also become obsolete, of course, but the test software shouldn't require any changes if this happens. An added benefit here is that the same test software will work on both a complex test fixture and a simple custom test setup without a fixture. With a layered design, test software can run in the factory on a multi-product tester with an automated fixture, and it can run in the field or at a repair location that requires minimal automation.

At this point, any astute test engineer would probably point out that I could have used the IVI (Interchangeable Virtual Instrument) specification, which was in its infancy in 1995, as a way to provide for reusable software. IVI works fine for test systems with individual instruments directly connected to the DUT (device under test), but it falls flat when a switching topology changes from, say, a VXI-C switch to an Agilent Technologies 34980A multifunction switch. IVI drivers can work in this design, but they can't take direct calls from the test software.

The project's second goal was to allow for an easy transition to a different software platform should the chosen software platform ever become obsolete. Keep in mind that a good software design, with good documentation, will let a good software engineer implement it in just about any software language in a short time.

The basic software design in **Figure 1** lets a test engineer change the hardware and only change hardware drivers. That provides full reuse of all the actual test software itself. In my implementation, I had all my own instrument drivers, so I combined the abstraction layer with the instrument drivers, which simplified the design.

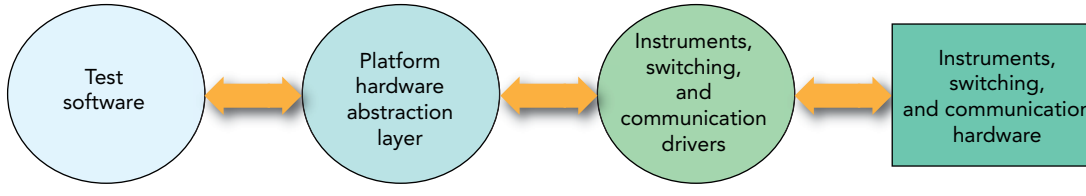

FIGURE 1. Modular software separates test functions from operating systems and hardware.

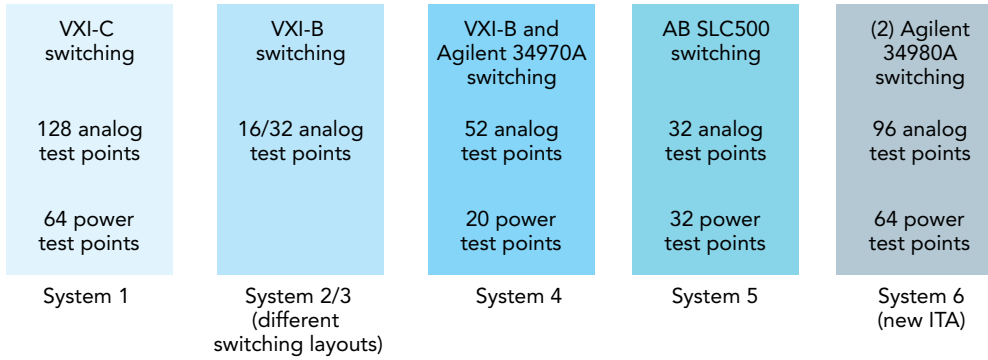

FIGURE 2. Software can be reused across several test systems, minimizing development time and cost.

Actual hardware implementations

The software design was deployed on six functional test platforms and two hipot test platforms. The main differences were in the switching. In one case, a different ITA was used; in two cases, a combined switch-and-measurement system replaced a DMM (digital multimeter) and separate switches.

The products tested on the smaller systems could also be tested on the larger systems, but not vice versa. Hewlett-Packard (now Agilent) designed and built System 1 and its ITA (**Figure 2**). I developed the original software for System 2 and ported it back to System 1.

For each new platform, I just created new platform switch drivers that let us reuse the software. This was especially beneficial on System 5, which had no development budget and for which I used a low-cost PLC (programmable logic controller) and I/O for all the switching. Because of the software design, I had to do almost no software-development work. System 5 would have been impossible to budget if there had been no platform abstraction layer.

I designed System 6 to use the latest switching and various other instruments. Since management wanted to replace the older systems and the fixtures, test engineers designed a new ITA that was simpler to wire than previous ITAs and had features that older systems lacked. Because the test software was reusable, System 6 needed testers and fixtures only.

The first of the hipot testers used Associated Research equipment with one to four 16-point switch units. The second used a Chroma (basically a QuadTech) hipot with eight built-in switch points. The Chroma job was part of the no-budget project. For this project, I needed two more hipot test points and used a PLC to control some discrete high-voltage relays. The switch driver was designed to know which instrument to send the switch commands to, according to the high-voltage relay number; the test software didn't know the difference.

Abstracting the ITA

We used two steps to design the ITA software. First, we assigned a logical name to every point on the ITA, such as ATP1 (analog test point 1) or PTP23 (power test point 23). The ITA also included digital test points, relays, and communications test points, but they weren't switched to different instruments.

We designed the platform interface to pass "connect" and "disconnect" commands to the switches using ITA logical names and the logical names of the instrument. For example, the system uses names such as DMM1_HI or DC1_LO. The code would pass the right commands to each instrument to make or break the connection. In the case of the DMM, since it was only allowed to connect to one test point at a time, it had an option to automatically disconnect the previous connection if a new connect command came without a disconnect command preceding it. This saved the developers a lot of headaches by forcing mutually exclusive use of the ATPs.

Second, we mapped the DUT to the ITA points so the test software could request DMM1_HI to connect to DUT OUTPUT1_HI and so on. The DUT names could be anything, including logical names or terminal numbers such as J1-1. This simplified the test coding and eliminated the need for the test engineer to know anything about the switching topology; it also made the test software easy to read and comprehend.

The key to success was the use of HP VEE (now Agilent VEE PRO) development environment. It was very text based and simple to use. I used ASCII files for the configuration data and test sequence files for each product, and I developed my own test executive designed around the business's Quality Information System data requirements. Each entry in the test sequence file textually called any test library function with any set or quantity of parameters, which made changes, experiments, and corrections to sequences faster than lightning (there was nothing to compile or link).

I wrote drivers for all the instruments and then put together the generic interface to the switching and the DUT followed by a high-level switching driver to sort out the connect requests and send them to the right switches on the right switch card on the right instrument.

When System 2 came out in 1997, I had the layered software working and kept improving it from there. With the development time it saved, I estimate my productivity increased tenfold.

I strongly recommend this idea to any business that uses complex testers that incorporate a lot of switching. It can be even more valuable if there are already multiple test platforms running different software sets to test the same products. As remote repair sites proliferate, requiring low-cost testers, it can only add value to the business. T&MW

Rob Marquardt *currently works as an independent test engineer. He has 30 years of experience designing test equipment, test software, and test executives. He holds a BSEE from the Milwaukee School of Engineering. ramarquardt@tds.net.*

Bridge software and hardware to accelerate SOC validation

System-on-a-chip debug and verification requires an understanding of hardware and software relationships

BY BRAD QUINTON, TEKTRONIX

SOCs (systems-on-a-chip) have progressed to the point where they now include a complex mix of software, firmware, embedded processors, GPUs (graphics processing units), memory controllers, and other high-speed peripherals. This increased functional integration, combined with faster internal clock speeds and complex, high-speed I/O, means that delivering a functional and fully validated system is harder than ever.

Traditionally, software validation and debug and hardware validation and debug have existed in separate worlds. Often, software and hardware teams have worked in isolation, with the former concentrating on software execution within the context of the programming model, and the latter debugging within the hardware-development framework, where clock-cycle accuracy, parallel operation, and the relationship of debug data back to the original design is key. In theory, fully debugged software and hardware should work flawlessly together. But in the real world, that rarely happens, a fact that often leads to critical cost increases and time-to-market delays.

To deliver increased integration within a reasonable cost and time, the industry must use a new approach: "design for visibility." Said another way, engineers must design—up front—the ability to deliver a full system view in order to permit effective validation and debug of SOCs. Engineers need to be able to understand causal relationships between behaviors that span hardware and software domains.

At Tektronix, we have developed an approach to debugging an SOC that makes use of embedded instruments, and we have found that integrating the hardware and software debug views can lead to faster and more efficient debug of the entire system.

Building the test bed

The test bed SOC shown in **Figure 1** is composed of a 32-bit RISC instruction set processor connected to an AMBA (advanced microcontroller bus architecture) AHB (advanced high-performance bus) and an AMBA APB (advanced peripheral bus). The SOC also contains a DDR2 memory controller, a Gigabit Ethernet network adapter, a CompactFlash controller, a VGA controller, and a number of low-speed peripheral interfaces. The SOC runs the Debian GNU Linux operating system version 4 running kernel v2.6.21. The processor core operates at 60 MHz, the DDR memory controller at 100 MHz, and the other I/O peripherals operate at their native frequencies between 33 MHz and 12 MHz. The entire SOC is implemented on a Virtex-5 development board.

Together, this system is a fully functional computer that can provide terminal-based user access, connect to the Internet, run applications, and mount file systems. Such an SOC creates complex debug scenarios and stresses the capabilities of both hardware and software debug infrastructures. In most cases, key operations span hardware and software.

Debug infrastructures

Developers of processor cores generally provide debug infrastructures, either as a fixed set of features for a given core or as a configurable add-on to a family of cores. In either case, the debug infrastructure becomes a part of the manufactured core. Debug software then uses this infrastructure to provide debug features to software developers.

The processor core supports a basic set of debug capabilities similar to those available on most modern processors, including those from Intel, AMD, IBM, Oracle, and ARM. In this case, a "backdoor" that is accessible via the JTAG bus allows a software debugger, for example GDB (GNU Debugger), to read and write memory in the system and detect the operational state of the processor. Because of this, and because they also have access to the original software source code, GDB and other software debuggers can provide software breakpoints, single-step operation, examina-

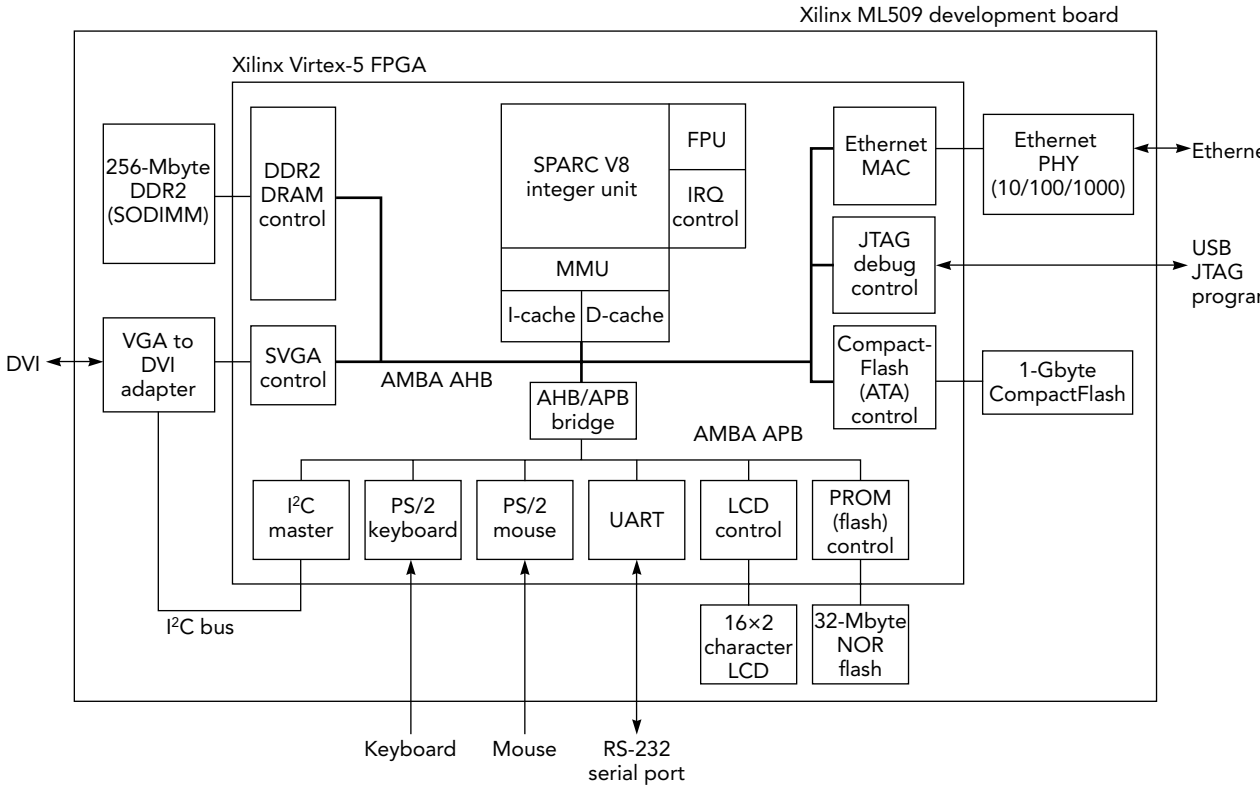

FIGURE 1. A test bed SOC contains the components of a complete computer capable of connecting to the Internet.

tion of variable values, stack tracing, configuration of initial conditions, alternation of memory values, and resume functionality.

In most cases, hardware debug infrastructures are not delivered with the hardware IP cores that make up an SOC. Instead, the hardware debug infrastructure is often overlaid onto an existing SOC design. There are a number of reasons for this difference. First, unlike in software debug, the underlying functionality required of hardware debug is diverse and often not completely understood until the SOC is assembled. Second, each new SOC often requires a different debug infrastructure.

Finally, because hardware debug is an emerging area, it has less standardization and less of an ecosystem. Thus, the development of a hardware debug infrastructure is often left to individual designers who create ad hoc debug features targeting different functional areas. Larger organizations often develop internally supported tools and architectures, but as the complexity of SOCs continues to rise, so does the complexity of creating an efficient hardware debug infrastructure, and internal development efforts become difficult to sustain.

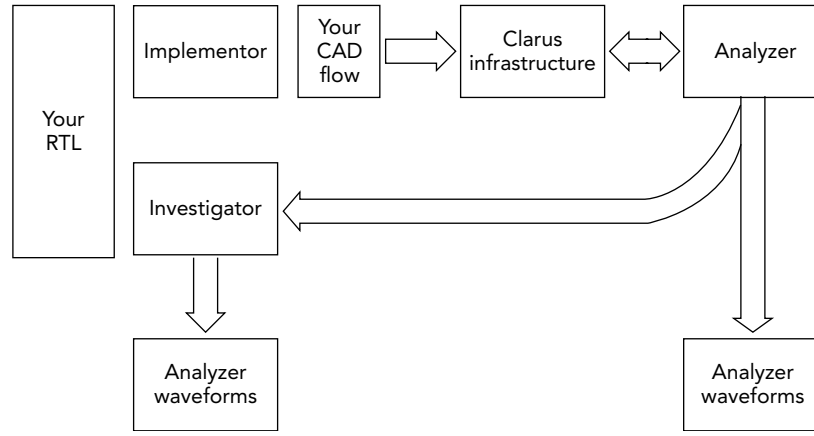

FIGURE 2. Configurable embedded instruments (Clarus Analyzer, Implementor, and Investigator) form a software debugging infrastructure.

As an alternative, test and measurement vendors can provide complete design tools, an IP library, and a work flow that make it easier for engineers to create a hardware debug infrastructure. The setup shown in **Figure 2**, our Clarus Post-Silicon Validation Suite, is composed of reconfigurable embedded instruments that can be connected and distributed throughout the SOC to create a debug infrastructure that is specific to the functional requirements. *(continued)*

The Clarus Implementor tool allows the instrumentation of any signal, at any level of hierarchy, at the RTL-level (Verilog, System Verilog, and VHDL) in the hardware design. The Clarus Analyzer configures and controls the embedded instruments over a JTAG or an Ethernet connection. Finally, the Clarus Investigator maps the data collected by the embedded instruments back to the original RTL (in a simulation environment) to permit a more complex debug.

The embedded instruments are applied to an SOC to provide a debug infrastructure as shown in **Figure 3.** An important aspect is the ability to reconfigure the instrument to target various signals and scenarios in different areas of the SOC while debug is in progress. The base instruments are called capture stations, which independently manage the selection, compression, processing, and storage of observed data. Multiple stations are often used to create a design-specific infrastructure for a given SOC.

During insertion, the capture stations are configured with a list of potential signals of interest, a maximum number of simultaneous observations, and a maximum RAM size. Capture stations are generally assigned to specific clock domains and capture synchronously to observed data. The Analyzer collects the data from each station, reverses the compression algorithms, and aligns the data captured in each station to produce a time-correlated view across all capture stations.

The SOC used in this example has four capture stations. Capture Station 1 (60 MHz), located in the processor clock domain, targets 362 signals. Capture Station 2 (25 MHz), in the RX Ethernet domain, targets 17 signals. Capture Station 3 (25 MHz), in the TX Ethernet domain, also targets 17 signals. Finally, Capture Station 4 (33 MHz), in the CompactFlash clock domain, targets 178 signals. Each of these stations operates in parallel and is able to make selective observations of any combination of signals. The final output of the Analyzer tool is a waveform representing the clock-cycle-accurate signal transactions in the actual silicon device (**Figure 4**).

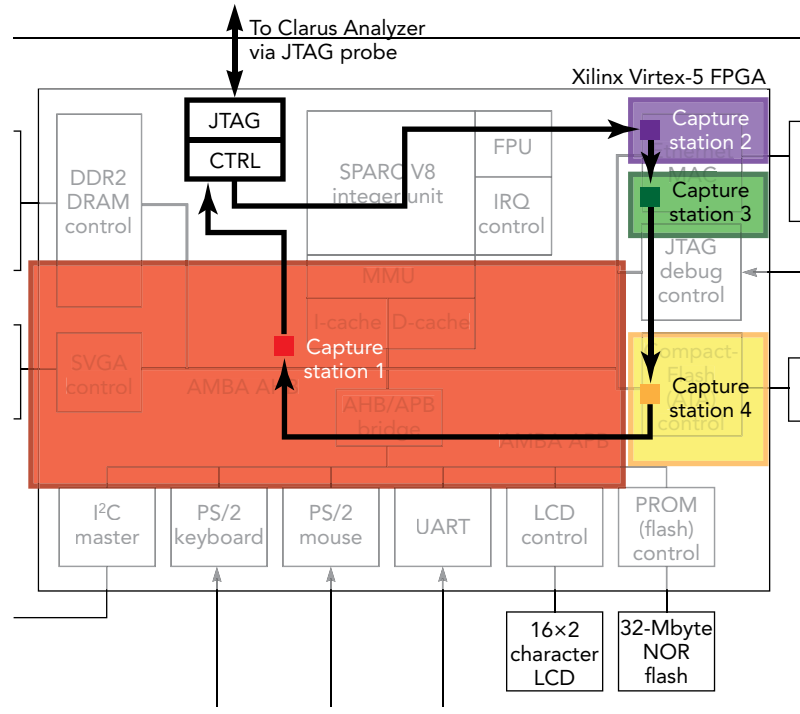

FIGURE 3. A hardware-debug infrastructure consists of capture stations that provide access to the SOC hardware; this figure illustrates the debug architecture superimposed over the FPGA portion of the test bed SOC in Figure 1.

SOC debug and event management

Both the software and hardware debug infrastructures perform well on the target platform for issues that are confined to either software or hardware, but engineers can still find it challenging to understand behavior that involves the interaction of software and hardware. **Table 1**

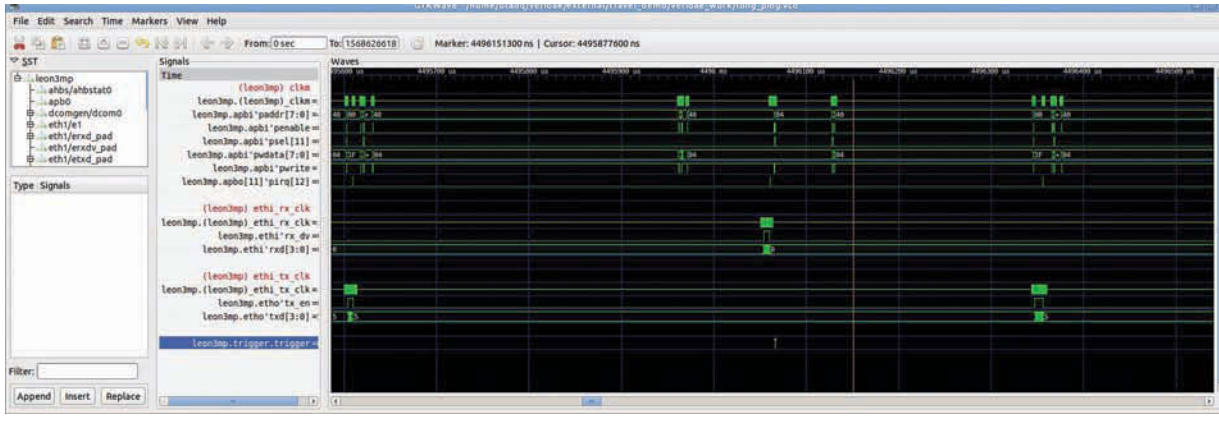

FIGURE 4. The analyzer produces an SOC waveform display.

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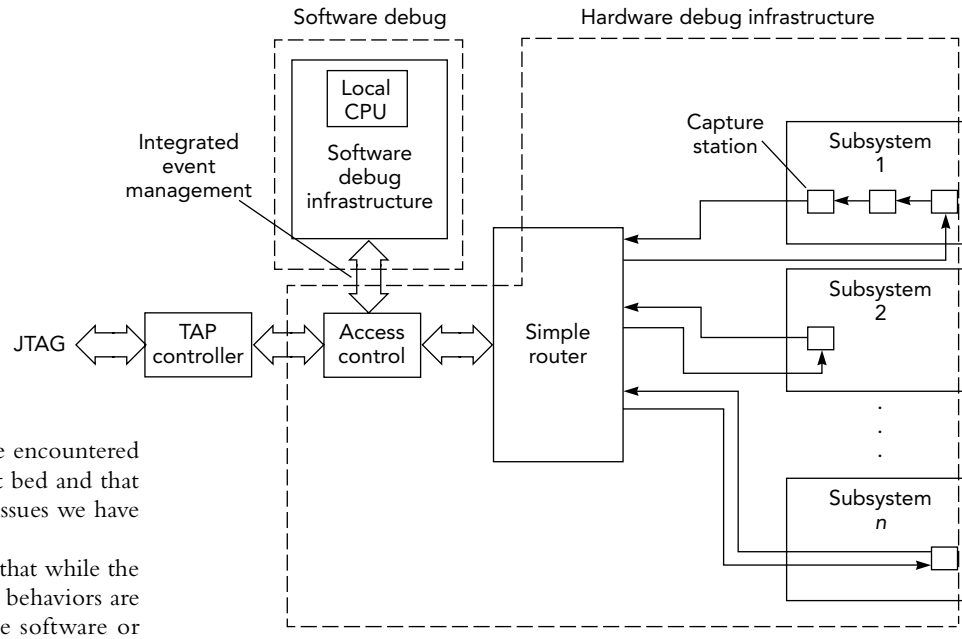

FIGURE 5. Distributed, asynchronous instruments let you view each capture station.

lists some of the issues we encountered when developing our test bed and that are representative of the issues we have seen across the industry.

A primary challenge is that while the effects of the unexpected behaviors are "visible" using either the software or hardware debug infrastructures, it can be difficult to determine whether the observed incorrect behavior is the cause or the symptom. The question often becomes: Was the unexpected behavior in the software a reaction to incorrect hardware behavior, or was it the other way around? The key is to determine the causal relationship between events, which requires a common reference between the software and hardware debug views.

The ability to reconstruct a causal relationship between software and hardware debug views requires "integrated event management," or the integration across the debug state and event processing from the two debug infrastructures (**Figure 5**). In this example, distributed, asynchronous instruments provided by the Clarus Suite make it possible for each capture station to be viewed as autonomous. A shared event bus and a centralized event processor (labeled "Access control") support "cross-triggering" between instruments. The Access control event processor communicates the debug events and state to the Analyzer software that manages the overall debug infrastructure. This enables the simultaneous hardware debug of many functional units and clock domains.

To create the integrated event management, this information propagates into and collects data from the software debug infrastructure. With integrated event management in place, the infrastructure can detect software breakpoint events and the debug state of the processor. Likewise, the software debug infrastructure is able to detect hardware triggers and the debug state of the hardware debug infrastructure.

The two key benefits of integrated event management are the ability of software-debug-initiated events to control hardware triggers and the ability of hardware-debug-initiated events to control software debug. More specifically, software breakpoints can be mapped to specific hardware behavior, and hardware triggers can break software at a specific point. Examples of these scenarios are shown in **Figures 6** and **7** in the online version of this story at www.tmworld.com/2012_04 (the figures are too large to reproduce adequately in print).

To demonstrate the capabilities of the software-initiated breakpoints in an integrated debug system, we modified the Linux kernel to print the message

Table 1: Example SOC debug issues

Issue #	Unexpected system behavior	Software "view"	Hardware "view"	Final resolution
1	Segmentation fault during boot.	"Random" segmentation faults.	Processor reads boot flash as normal and then halts.	Critical path timing violation causing data corruption.
2	"Lockup" during Ethernet initialization.	Ready bit fails to assert.	Processor reads same location repeatedly.	Orphan state in Ethernet MAC caused when start-up in 10-MHz mode.
3	DHCP request fails.	No Ethernet connectivity.	Transmit packets, but no response packets.	ESD (electrostatic discharge) issue caused marginality on Ethernet PHY timing.
4	Failure to mount CompactFlash "disk."	No response from read requests to CompactFlash controller.	Corrupt responses/lockup from external controller.	External CompactFlash controller not reset, correction reboot.
5	Shutdown command fails.	Shutdown command proceeds and then lockup occurs.	Normal operation and then no new transactions issued.	CompactFlash disk full because of excessive logging during shutdown.

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"BLOCK" when a read occurs on disk sector 0x00041d90. Then, we targeted traces from the "sysace" CompactFlash controller with the debug infrastructure. Using GDB, we set a hardware breakpoint on line 714 of the xsysace.c file (the line where the printk occurs). Then, we configured the test infrastructure to monitor the software debug infrastructure using integrated event management. Finally, the "find /" command forced the kernel to read the entire disk.

The software breakpoint halted kernel execution on the desired line and also triggered the hardware debug infrastructure. As a result, the detailed behavior of the hardware is visible at the time of the software breakpoint.

We used the Ethernet adapter to demonstrate the capabilities of the hardware-initiated triggers in an integrated debug system. We set a hardware trigger to occur when the "RX Packet Ready Interrupt Bit" in the Ethernet adapter was cleared by the Linux kernel. We configured the integrated event-management interface to map hardware events to the software debug infrastructure.

A ping to the IP address of the router in the system initiated a transmit packet from the SOC, to which the router responded. When that response occurred, the packet arrived on the Ethernet PHY and was processed by the Ethernet adapter. The processor was then interrupted, and the Linux kernel serviced the interrupt. When the interrupt servicing was complete, the interrupt was cleared. This caused a hardware trigger and the software halted. The resulting view shows the simultaneous or time-correlated behavior of hardware and software in a complex system from the PHY level all the way to the operating system.

The use of an integrated event-management interface between software and hardware debug infrastructures permits single-event synchronization that enables the meaningful presentation of simultaneous debug data from both infrastructures. Such a full system view opens a window into the causal relationship between SOC functionality that spans software and hardware, leading to faster and more efficient debug of increasingly complex SOC designs. T&MW

FOR MORE INFORMATION

See the online version of this article for Figures 6 and 7. www.tmworld.2012_04.

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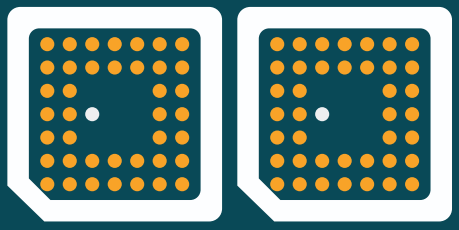

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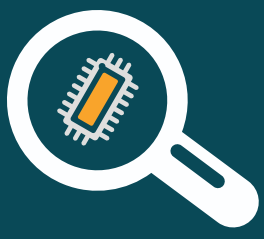

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Find out why LCDs Fail

The combination of SEM and EDX techniques reveal why inactive lines sometimes appear in liquid-crystal display screens.

BY MARK WOOLLEY AND JAE CHOI, AVAYA

The TFT (thin-film transistor) LCD devices found in so many products are manufactured using semiconductor processes that deposit materials on a glass substrate. Because of their small size, TFT LCDs are subject to many of the same failure modes as semiconductor ICs. Two methods of inspecting TFT displays, those using SEM (scanning-electron microscopy) and EDX (energy-dispersive x-ray spectroscopy) techniques, typically analyze surfaces only. The penetration depths of their electron beams are limited.

When the column voltage is high enough, however, penetration of electrons can reach 1 µm into the materials. Often, that's deep enough for you to determine the composition of an under layer's materials. Used in combination, SEM and EDX technologies can help you determine the cause of a failure.

An SEM produces black-and-white images using electrons generated in a reaction with the electrons in the source beam. The images show basic topology, but they contain little information about the elements present. The simultaneous use of an EDX detector can indicate what elements are present in the sample as well. Combining these two technologies can be useful in determining the cause of a failure.

Color TFT LCD displays are manufactured using layers of metal that form conductors on the glass. The conductors carry voltages and currents to the source and gate of each TFT in the viewing area. To reduce the number of conductors, the TFTs sources are connected in vertical columns while the gates are connected in horizontal rows. Individual pixels are turned on through scanning techniques.

The gate conductors are routed along the bottom of the glass panel, toward the left and right edges, and then along the edges to the appropriate row of transistors in the viewing area. The source conductors for the transistors are routed nearer the center of the glass panel and connect the sources in vertical columns. That makes the TFT's gate conductors longer than the source conductors, and the conductors are located more peripherally on the display glass panel. Because of this arrangement, the gate conductors are more susceptible to damage than the source conductors.

A visual inspection can detect defects in the conductors that are related to the inactive rows of pixels. **Figure 1** shows an area of conductors that carry signals to the TFT gates. Although multiple conductors have damage, each damage location affects only one conductor. A sharp instrument could damage multiple conductors, but the damage would be in a continuous line, not scattered as seen in this image.

Each conductor in Figure 1 is 5 µm wide. The damage was very localized, indicating that it could not have been caused by a pair of tweezers, because tweezers are much larger.

SEM analysis and EDX mapping

To produce the image of the damage, we used an SEM system with a 20-keV beam energy. The 20-keV beam causes electrons to penetrate approximately 1 µm below the surface. Two areas were selected for further analysis. The area shown in **Figure 2** has obvious damage in the passivation layer that covers the

FIGURE 1. An optical image shows damaged conductors in an LCD.

conductors. (This SEM image was constructed from secondary electrons.)

Figure 3 shows an anomalous region of a conductor that is darker than its neighbors. We analyzed this site because of the anomaly. The SEM found no damage to the passivation layer over the conductor. Only the conductor had been affected.

We next applied EDX mapping to the area shown in Figure 2. The main elements we detected were silicon, aluminum, and molybdenum. We made maps for these three elements at a lower magnification. **Figure 4** shows the image captured and the elemental maps.

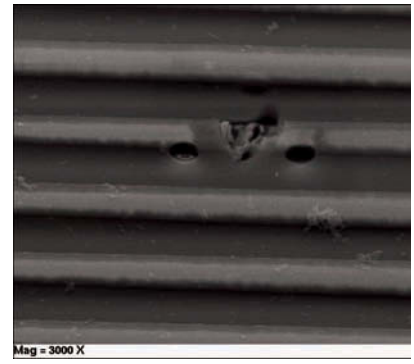

FIGURE 2. A 20-keV beam lets electrons penetrate approximately 1 µm below the surface, revealing damage.

We gleaned several pieces of information from this image:

- The entire panel is manufactured on glass. The elements present in the glass are silicon, calcium, oxygen, and sodium. We excluded oxygen from the map because it is also in silicon dioxide. In mapping this area, we did not note any sodium or calcium. The lack of these elements suggests that the manufacturer coated the glass with a passivation layer (SiO_2) before starting to build the metal conductors.
- The aluminum and molybdenum are mapped as white dots on the display. The brighter the area, the greater abundance of x-rays specific to these elements.
- The aluminum map shows a long stretch of conductor that is missing aluminum, beginning at the damaged site and extending to the right in the map.
- Molybdenum is less bright than aluminum, because the element's characteristic x-rays aren't generated as easily under these conditions. There is, however, a definite area at the damage site that is nearly devoid of molybdenum.
- A silicon map shows that the amount of silicon detected is greater between the conductors. The metal in the conductors dramatically reduces the penetration of the electrons to the silicon beneath them. Only the silicon in the passivation layer on top of the conductors is imaged. Between the conductors, the electrons can penetrate through the top passivation layer into the passivation layer deposited on the glass.
- A bright area in the silicon map is co-located with the missing aluminum. This indicates that the aluminum metallization is missing in this area, allowing the electrons to penetrate deeply into the bottom passivation layer.

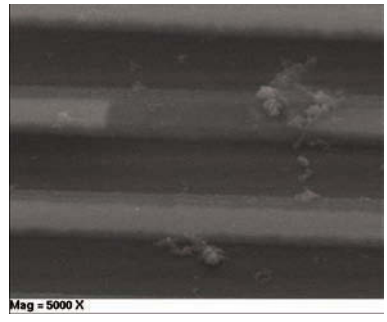

FIGURE 3. An anomalous area in a conductor is darker than neighboring areas.

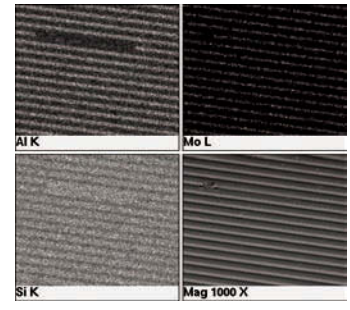

FIGURE 4. Elemental maps magnified 1000X let you analyze material composition.

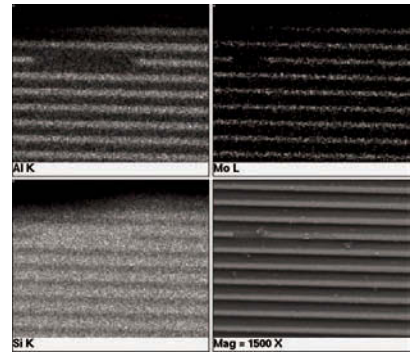

FIGURE 5. SEM did not show the TFT damage in Figure 3, but EDX techniques did.

We then applied EDX mapping to the area shown in Figure 3. The results appear in **Figure 5.** Using the same logic as above, we made the following conclusions:

- We noted no damage to the top layer of passivation in the damaged area.
- There is a relatively long section of missing aluminum.
- A much smaller section of the conductor lacks molybdenum as well.
- The molybdenum alone does not prevent electron penetration, so the layer is thin.

Passivation damage can occur for a variety of reasons, including particulate contamination during the deposition, imaging, and etch processes, or during the subsequent manufacturing operation necessary to produce a display. It may even occur as a result of thermal damage. SEM alone can show that much, but SEM alone did not show us what was occurring in Figure 3, where there was an open circuit but no damage to the passivation.

These failures were probably built into the product during the deposition of the metallization layer on the glass panels. Creating metal conductors requires several cycles of metal deposition, photoresist application, imaging, and development, as well as wet chemical etching. At any of these steps, problems with the adhesion of the photoresist or etching of the metal beneath the resist would create these apparent gaps in the conductor. T&MW

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Jae Choi, *PhD, is the manager of the laboratory at Avaya. He has written several papers on the polymerization and manufacturing of plastics.*

SPECIAL FOCUS: Probes

Tek probes designed for high voltages

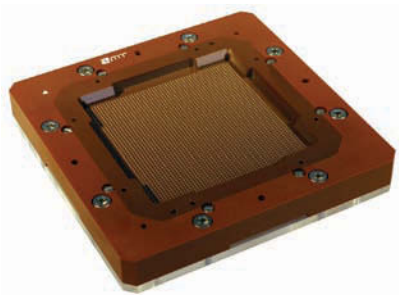
The Tektronix THDP, TMDP, and P52xxA high-voltage probes offer what the company says is an unmatched combination of bandwidth, dynamic range, and input impedance. The 200-MHz THDP0200 and TMDP0200 probes capture signals with fast slew rates to enable accurate power measurements. The 100-MHz THDP0100 offers ±6000-V differential and common-mode specifications, while the 100-MHz P5202A offers low attenuation and an excellent signal-to-noise ratio. In addition, the P5210A and the THDP0100 probes offer resistance of 40 MΩ and capacitive loading of less than 2.5 pF.

Base prices: 200-MHz TMDP0200 probe—$1690; 50-MHz P5200A probe—$899. *Tektronix, www.tek.com.*

Contactor handles large digital arrays

Based on Multitest's Quad Tech vertical-contact probe technology, the Triton contactor can be used to test the large grid-array packages typically found in high-end digital applications, such as smartphones and servers. Triton offers a differential bandwidth of up to 20 GHz, suitable for the next generation of these highly integrated digital devices.

Triton solves the challenges introduced by contactor bowing, limited compliance, and test-handler force limitations by offering an enhanced compliance window to accommodate stack-height variations, an optimum force to support large BGAs and LGAs, and multisite package test.



The Triton production-test contactor works with grid-array packages with pitches down to 0.4 mm. It also allows the use of a floating alignment plate and can be used for singulated testing, strip testing, or wafer-scale testing. Triton operates over a temperature range of −55°C to +155°C. Typical probe life is 500,000 cycles.

Multitest, www.multitest.com.

LeCroy probe works with PCIe protocol analyzers

LeCroy has introduced a multi-lead probe for its Summit T3-16 and T3-8 protocol analyzers. The new probe supports PCI Express 3.0, and is expandable to support from x1 to x16 PCI Express lanes when used with a Summit protocol analyzer. The probe tips are flexible for tapping signals in narrow areas on circuit boards, and the probe head uses LeCroy's Gen3 tapping technology, which offers precision signal tapping for 8 GT/s.

LeCroy, www.lecroy.com.

R&S LTE RF system verifies location-based services

The TS8980LBS LTE RF test system from Rohde & Schwarz allows manufacturers of mobile wireless devices to perform preconfigured conformance tests to ensure that location-based services such as LPP (LTE positioning protocol) work properly. This scalable platform not only supports conformance testing of international location-based services, but also performs protocol tests and network-operator test cases that combine data-transmission tests and position location.

Customers who already use the TS8980 simply need to add the SMBV100A signal generator equipped with the LBS software.

Rohde & Schwarz, www.rohde-schwarz.com

Sakor unveils HEV tester

Sakor Technologies has released a user-configurable test system for HEV (hybrid/electric vehicle) drivelines and vehicle subsystems. The system runs various road load profiles and simulations, performing tests to all international standards. The platform combines a high-voltage battery simulator, one or more AccuDyne AC motoring dynamometers, and a DynoLAB EM data-acquisition and control system. It can be adapted for R&D, performance evaluation, and durability testing of electric motors and inverters, high-voltage batteries, and transmissions.

Sakor Technologies, www.sakor.com.

LinkRunner AT checks Ethernet connectivity

With the touch of a button, the LinkRunner AT from Fluke Networks performs six Ethernet connectivity tests and returns results in less than 10 s. The LinkRunner AT also lets users create a custom test methodology, and it enables technicians to automatically perform a standardized set of tests, reducing errors and speeding problem resolution.

The unit can instantly verify the signal and link integrity of connections at 10 Mbps, 100 Mbps, and 1 Gbps on copper or fiber, and it stores up to 50 test results for downloading to a PC. The six connectivity tests it performs are continuity, link speed and duplex, DHCP and DNS server availability and performance, ping and TCP port connectivity using IPv4 and IPv6, nearest switch and port identification, and PoE loading (copper only).

Fluke Networks, www.flukenetworks.com.

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[An exclusive commentary from a technical leader]

LARRY DESJARDIN
Contributing Editor

Larry Desjardin is the founder and president of Modular Methods. He joined Hewlett-Packard (now Agilent Technologies), serving in several R&D and executive management positions. As an R&D manager, he received the John Fluke Sr. Memorial Award in recognition of his contribution to the creation of the VXIbus. Most recently, he was GM of Agilent's Modular Product Operation before retiring in 2011. Desjardin is also the author of the "Outside the Box" blog on www.tmworld.com. He holds a BSEE from CalTech and an MSEE from Stanford University.

Read Larry Desjardin's complete report from the Mobile World Congress: bit.ly/yd7ck2

Nontraditional test at MWC

I recently had the pleasure of reporting from MWC (Mobile World Congress) in Barcelona for *Test & Measurement World* (bit.ly/yd7ck2). Why is MWC important to readers of *T&MW*? It's simple: Wireless communications is the largest macro segment in test and measurement. My impressions from MWC led me to conclude that the largest technology drivers for test are MIMO, LTE, LTE-Advanced, 802.11ac, and WiGig.

MIMO threads its ways into all the other technologies and requires multichannel test architectures that are phase coherent for signal generation and reception. LTE and LTE-Advanced are driving the cellular industry. A year from now, expect tablets, handsets, and base stations to routinely support the standard. 3G will remain the only true international roaming standard for wireless data. Domestically, providers will slowly coerce customers to adopt 3G-capable phones to replace 2G models to free up spectrum.

Nonlicensed technologies like Wi-Fi will play a role as well. It's all about bigger, faster pipes like 802.11ac and WiGig, each of which presents challenges to instrumentation, in both bandwidth and spectrum range.

Nontraditional test methods will be essential for mobile test. Modular instrumentation certainly was alive and visible at MWC. Aeroflex is offering both modular and traditional box solutions by packaging its PXI RF modules into box instruments, complete with buttons, knobs, and displays, and it makes use of the same measurement science software on all platforms.

Agilent Technologies' N7109A signal analyzer showed phase-synchronous measurements for TD-SCDMA and LTE-Advanced. The N7109 is a "nearly PXI" architecture that shows the size reduction possible by modular: eight channels in a single chassis.

National Instruments is also making a major push into RF instrumentation. Company CEO Jim Truchard ("Dr. T") listed a number of factors that made RF a favorable market for NI, including the short development time of applications in LabView and the ability for users to program at the FPGA level for fast DSP and other algorithms. Another point Dr. T brought up was all the testing that occurs around a smartphone. The display, audio, accelerometers, GPS, and battery are all examples of integrated technology, and all require testing. Dr. T's point was that a cellphone is not merely RF, but all of these functions together, and PXI has a proven track record of testing those.

Modular architectures were not limited to PXI. Tektronix and EXFO showed network monitoring and simulation solutions based on the AdvancedTCA standard that is widely used in telecom networks. To be sure, traditional box instrumentation still dominates physical-layer testing for RF, but just a few years ago, modular solutions were at 0%.

But nontraditional testing is not just modular. Another example is the emergence of "nonsignaling" test for handsets. In traditional functional test, the DUT (device under test) is exercised exactly like it will be used in its final environment. For a handset, that means emulating a base station and making phone calls to test all the bands and functions. The signaling between the handset and base station takes a good portion of the test time but adds little value. Nonsignaling test puts the DUT into a special mode where the physical tests are quickly sequenced in a defined order. At MWC, Altair Semiconductor indicated dramatic decreases in test times. Products like the Rohde & Schwarz CMW500 and Agilent EXT wireless testers take advantage of the special test sequences, as do some PXI-based options.

Probably the most interesting nontraditional test I saw at MWC was the PacketPortal probe from JDSU. JDSU designed the measurement probe, a tiny ASIC, into a standard optical package that is inserted into any optical Gigabit Ethernet node of the network. The probe becomes part of the DUT itself—the DUT being an entire telecom network. The solution's value is in its scalability: It can be widely deployed at the edge of the network, exactly where the creative new services are being deployed. T&MW

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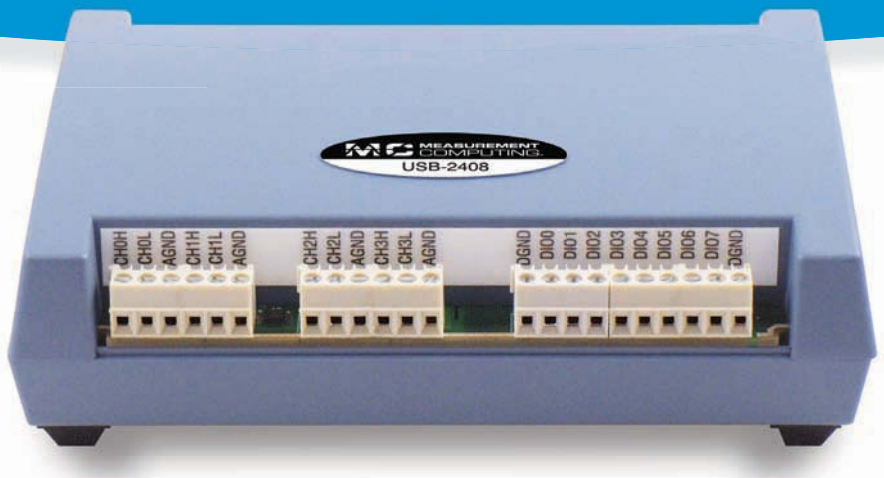

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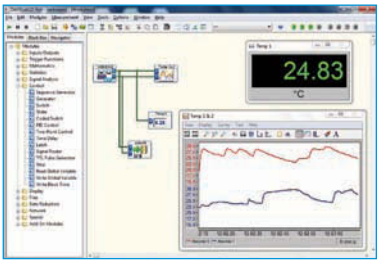

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